What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A low profile ball grid array semiconductor package comprising:

a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface;

a thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed; and

a semiconductor element mounted in said cavity.

2. The low profile ball grid array semiconductor package according to claim 1, said thin sheet material further comprising:

a polyimide based material having a thickness of approximately 0.025 to 0.1 mm.

3. The low profile ball grid array semiconductor package according to claim 1, said thin sheet material further comprising:

a metal foil based material having a thickness of approximately 0.025 to 0.1 mm.

4. The low profile ball grid array semiconductor package according to claim 1 further comprising:

an encapsulant covering at least a portion of said semiconductor element and said base substrate.

5. A low profile ball grid array semiconductor package comprising:

a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface;

a series of conductive traces located on said bottom surface of said base substrate;

a plurality of conductive balls connected to said series of conductive traces;

a thin sheet material thick secured to said top surface of said base substrate and covering said aperture to form a downward facing cavity; and

a semiconductor element mounted in said downward facing cavity.

6. The low profile ball grid array semiconductor package according to claim 5, wherein said thin sheet material has a thickness in the range of approximately 0.025 to 0.1 mm.

7. The low profile ball grid array semiconductor package of claim 6, said thin sheet material further comprising:

a polyimide based material.

8. The low profile ball grid array package of claim 6, said thin sheet material further comprising:

a metal foil based material.

9. The low profile ball grid array package of claim 5 further comprising:

an encapsulant covering at least a portion of said semiconductor element and said base substrate.

10. A low profile ball grid ~~array~~ semiconductor package comprising:

an insulating substrate having a top surface and a bottom surface, said insulating substrate having an aperture extending from said top surface to said bottom surface;

a first series of conductive traces located on said top surface of said insulating substrate and a second series of conductive traces located on said bottom surface of said insulating substrate, said first series connected to said second series by via holes in said insulating substrate;

a thin sheet material approximately 0.025 to 0.1 mm thick secured to said bottom surface of said insulating

substrate and covering said aperture such that a cavity is formed;

a semiconductor element mounted in said cavity, said semiconductor element having a plurality of bond pads, each of said bond pads associated with an input or an output of said semiconductor element;

a plurality of wire bonds connecting said bond pads of said semiconductor element to said first series of conductive traces;

a plurality of conductive balls connected to said second series of conductive traces; and

an encapsulant covering at least a portion of said semiconductor element and said insulating substrate.

11. The low profile ball grid array semiconductor package of claim 10, said thin sheet material further comprising:

a polyimide based material.

12. The low profile ball grid array package of claim 10, said thin sheet material further comprising:

a metal foil based material.

13. A low profile ball grid array semiconductor package comprising:

an insulating substrate having a top surface and a bottom surface, said insulating substrate having an aperture extending from said top surface to said bottom surface;

a series of conductive traces located on said bottom surface of said insulating substrate;

a thin sheet material thick secured to said top surface of said insulating substrate and covering said aperture such that a downward facing cavity is formed;

a semiconductor element mounted in said downward facing cavity, said semiconductor element having a plurality of bond pads, each of said bond pads associated with an input or an output of said semiconductor element;

a plurality of wire bonds connecting said bond pads of said semiconductor element to said series of conductive traces;

a plurality of conductive balls connected to said series of conductive traces; and

an encapsulant covering at least a portion of said semiconductor element and said insulating substrate.

14. The low profile ball grid array semiconductor package according to claim 13, wherein said thin sheet material has a thickness in the range of approximately 0.025 to 0.1 mm.

15. The low profile ball grid array semiconductor package of claim 14, said thin sheet material further comprising:

a polyimide based material.

16. The low profile ball grid array package of claim 14, said thin sheet material further comprising:

a metal foil based material.

17. An integrated circuit comprising:

a plurality of low profile ball grid array semiconductor packages; and

a plurality of leads connecting said plurality of ball grid array semiconductor packages together to form a complete circuit, said low profile ball grid array semiconductor packages further comprising a semiconductor element mounted in a cavity on a thin sheet material approximately 0.025 to 0.1 mm thick.

18. The integrated circuit of claim 17, each of said low profile ball grid array semiconductor packages further comprising:

a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface, said thin sheet material being secured to said bottom surface of said base substrate to cover said aperture and form said cavity,

said semiconductor element being mounted in said cavity on said thin sheet material;

a first series of conductive traces located on said top surface of said base substrate and a second series of conductive traces located on said bottom surface of said base substrate, said first series of conductive traces being connected to said second series of conductive traces by via holes in said base substrate;

a plurality of bond pads on said semiconductor element, each of said bond pads associated with an input or output of said semiconductor element;

a plurality of wire bonds connecting said bond pads of said semiconductor element to said first series of conductive traces;

a plurality of conductive balls connected to said second series of conductive traces; and

an encapsulant covering at least a portion of said semiconductor element and said base substrate.

19. The integrated circuit of claim 17, each of said low profile ball grid array package further comprising:

a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface, said thin sheet material being secured to said top surface of said base substrate to cover said aperture and form said cavity

in a downward direction, said semiconductor element being mounted in said downward cavity;

a series of conductive traces located on said bottom surface of said base substrate;

a plurality of bond pads on said semiconductor element, each of said bond pads associated with an input or output of said semiconductor element;

a plurality of wire bonds connecting said bond pads of said semiconductor element to said series of conductive traces;

a plurality of conductive balls connected to said series of conductive traces; and

an encapsulant covering at least a portion of said semiconductor element and said base substrate.

20. A device for mounting a semiconductor element comprising:

an insulating substrate, said insulating substrate having a top surface and a bottom surface, with an aperture therein extending from said top surface to said bottom surface; and

a thin sheet material approximately 0.025 to 0.1 mm thick secured to said bottom surface of said insulating substrate and covering said aperture to form an upwards facing cavity,

wherein said semiconductor element is mounted in said cavity.

21. The device for mounting a semiconductor element according to claim 20, said thin sheet material further comprising:

a polyimide based material.

22. The device for mounting a semiconductor element according to claim 20, said thin sheet material further comprising:

a metal foil based material.

23. A device for mounting a semiconductor element comprising:

an insulating substrate, said insulating substrate having a top surface and a bottom surface, with an aperture therein extending from said top surface to said bottom surface; and

a thin sheet material approximately 0.025 to 0.1 mm thick secured to said top surface of said insulating substrate and covering said aperture to form a downwards facing cavity,

wherein said semiconductor element is mounted in said downwards facing cavity.

24. The device for mounting a semiconductor element according to claim 23, said thin sheet material further comprising:

a polyimide based material.

25. The device for mounting a semiconductor element according to claim 23, said thin sheet material further comprising:

a metal foil based material.

26. A printed circuit board comprising:

a plurality of low profile ball grid array semiconductor packages; and

a plurality of leads connecting said plurality of ball grid array semiconductor packages together to form a complete circuit, said low profile ball grid array semiconductor packages further comprising a semiconductor element mounted in a cavity on a thin sheet material.

27. The printed circuit board according to claim 26, wherein said thin sheet material has a thickness in the range of approximately 0.025 to 0.1 mm.

28. The printed circuit board according to claim 27, each of said low profile ball grid array semiconductor packages further comprising:

a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface, said thin sheet material being secured to said bottom surface of said base substrate to cover said aperture and form said cavity, said semiconductor element being mounted in said cavity on said thin sheet material;

a first series of conductive traces located on said top surface of said base substrate and a second series of conductive traces located on said bottom surface of said base substrate, said first series of conductive traces being connected to said second series of conductive traces by via holes in said base substrate;

a plurality of bond pads on said semiconductor element, each of said bond pads associated with an input or output of said semiconductor element;

a plurality of wire bonds connecting said bond pads of said semiconductor element to said first series of conductive traces;

a plurality of conductive balls connected to said second series of conductive traces; and

an encapsulant covering at least a portion of said semiconductor element and said base substrate.

29. The printed circuit board according to claim 27, each of said low profile ball grid array semiconductor packages further comprising:

a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface, said thin sheet material being secured to said top surface of said base substrate to cover said aperture and form said cavity in a downward direction, said semiconductor element being mounted in said cavity;

a series of conductive traces located on said bottom surface of said base substrate;

a plurality of bond pads on said semiconductor element, each of said bond pads associated with an input or output of said semiconductor element;

a plurality of wire bonds connecting said bond pads of said semiconductor element to said series of conductive traces;

a plurality of conductive balls connected to said series of conductive traces; and

an encapsulant covering at least a portion of said semiconductor element and said base substrate.

30. A method for fabricating a low profile ball grid array semiconductor package comprising the steps of:

providing a base substrate, said base substrate having a top surface and a bottom surface, with an aperture extending from said top surface to said bottom surface;

forming a cavity with said aperture and a thin sheet material; and

mounting a semiconductor element in said cavity.

31. The method for fabricating a low profile ball grid array semiconductor package according to claim 30, wherein said thin sheet material has a thickness in the range of approximately 0.025 to 0.1 mm.

32. The method for fabricating a low profile ball grid array semiconductor package according to claim 31, said step of forming a cavity further comprising:

securing said thin sheet material to said bottom surface of said base substrate to cover said aperture to form an upward facing cavity.

33. The method for fabricating a low profile ball grid array semiconductor package according to claim 31, said step of forming a cavity further comprising:

securing said thin sheet material to said top surface of said base substrate to cover said aperture to form a downward facing cavity.

34. The method for fabricating a low profile ball grid array semiconductor package according to claim 31 further comprising the step of:

encapsulating at least a portion of said semiconductor element and said base substrate.

35. A method for mounting a semiconductor die comprising the steps of:

providing a base substrate having a top surface and a bottom surface with an aperture extending from said top surface to said bottom surface;

forming a cavity by securing a support material approximately 0.025 to 0.1 mm thick to said base substrate to cover said aperture; and

mounting said semiconductor die in said cavity.

36. The method for mounting a semiconductor die according to claim 35, said step of forming a cavity further comprising:

securing said support material to said bottom surface of said base substrate to form an upwards facing cavity.

37. The method for mounting a semiconductor die according to claim 35, said step of forming a cavity further comprising:

securing said support material to said top surface of said base substrate to form a downwards facing cavity.

38. The method for mounting a semiconductor device according to claim 35 further comprising the step of:

encapsulating at least a portion of said semiconductor die and said base substrate.

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39. A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of ball grid array semiconductor packages, said ball grid array semiconductor packages comprised of an insulating substrate having a top surface and a bottom surface, said insulating substrate having an aperture therein extending from said top surface to said bottom surface,

a thin sheet material approximately 0.025 to 0.1 mm thick secured to said top side of said substrate to form a cavity, and a semiconductor die mounted in said cavity.

40. The processor system according to claim 39, said thin sheet material further comprising:

a polyimide based material.

41. The processor system according to claim 39, said thin sheet material further comprising:

a metal foil based material.

42. A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of ball grid array semiconductor packages, said ball grid array semiconductor packages comprised of an insulating substrate having a top surface and a bottom surface, said insulating substrate having an aperture therein extending from said top surface to said bottom surface,

a thin sheet material approximately 0.025 to 0.1 mm thick secured to said bottom side of said substrate to form a cavity, and a semiconductor die mounted in said cavity.

43. The processor system according to claim 42, said thin sheet material further comprising:

a polyimide based material.

44. The processor system according to claim 42, said thin sheet material further comprising:

a metal foil based material.